plurality of electronic devices coupled to a first half-capacitor attached to said chip; and,

a second half-capacitor attached to said substrate and capacitively coupling a signal to said first half-capacitor.

21 ~~44~~. (Amended) A modular electronic system [as defined in claim ~~41~~ 40 further] comprising:

a substrate;

a chip;

means for powering said chip;

means for capacitively signaling between said chips and said substrate comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap that is at least partially filled with a dielectric; and

a power connector extending through said dielectric.

22 ~~59~~. (Amended) A modular electronic system [as defined in claim 37 wherein said chip further includes] comprising:

a substrate;

a chip;

means for powering said chip;

means for capacitively signaling between said chips and said substrate comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap; and

an additional half-capacitor on its backside.

23 ~~102~~. (Amended) A modular electronic system comprising:

a first module having a plurality of electronic devices, [and] a first half-capacitor and at least one signal lead connecting said electronic devices to said first half-capacitor; and

a second module having a second half-capacitor, said modules being positioned such that said first and second half-capacitors provide a capacitive signal path between said first and second modules.

REMARKS

In the Office Action of August 25, 1997, the Examiner limited the claims for consideration to claims 1, 28, 37-48, 52-59, 102, 143, 144, 146 and 147. He indicated that claims 44 and 59 would be allowed if rewritten in independent form. He rejected claims 1, 28, 37-39, 41-43, 47, 52-57, 102, 143, 144, 146 and 147 under 35 U.S.C. §102(e) as anticipated by U.S. Patent 5,404,265 to Moresco et al. He rejected claims 40, 45, 46 and 48 under 35 U.S.C. §103(a) as unpatentable over Moresco.

A new title was requested and an abstract.

A request has been made to extend the time to respond for a period of three months to February 25, 1998.

In response to this Office Action, a new title and an abstract have been supplied; claims 44 and 59 have been rewritten in independent form; and independent claims 1, 28 and 102 have been amended. The rejection of the claims on Moresco is respectfully traversed.

Applicant's invention relates to an apparatus for communicating or signalling between chips, modules or substrates. For example, in large part, the need for multichip modules arises from the inability of the prior art to produce arbitrarily large semiconductor dies with acceptable yield as well as the high cost of wiring on semiconductor dies. Such problems have forced designers to partition large systems among multiple dies. To effect signalling between different chips and modules, the prior art requires the use of connectors, solder bumps, wire-bond interconnections or the like. Unfortunately, such means